(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 358 166 B1**

(12) EUROPEAN PATENT SPECIFICATION

(45) Date of publication of patent specification: **13.07.94**

(51) Int. Cl.5: **H04B 1/38**, H04M 1/72, H04B 1/16

(21) Application number: **89116369.3**

(22) Date of filing: **05.09.89**

(54) Power saving arrangement and power saving method.

(30) Priority: **07.09.88 JP 224038/88**

(43) Date of publication of application:
14.03.90 Bulletin 90/11

(45) Publication of the grant of the patent:
13.07.94 Bulletin 94/28

(84) Designated Contracting States:
DE FR GB

(56) References cited:
EP-A- 0 091 695
EP-A- 0 234 201
GB-A- 2 114 343
US-A- 4 194 153
US-A- 4 384 361

(73) Proprietor: **SANYO ELECTRIC CO., LTD.**
18, Keihanhondori 2-chome
Moriguchi-shi Osaka-fu(JP)

(72) Inventor: **Ishiguro, Kazuhisa**
183-42, Kizaki Nittamachi
Nitta-gun Gunma(JP)
Inventor: **Sekiguchi, Yutaka**
1-219 Ootone-Ryo 611, Yorikido
Ooizumimachi Oora-gun Gunma(JP)

(74) Representative: **Glawe, Delfs, Moll & Partner**
Patentanwälte
Postfach 26 01 62
D-80058 München (DE)

EP 0 358 166 B1

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to a power saving arrangement and power saving method for use in a subsidiary unit, such as a handset unit, which communicates with a base unit in response to the detection of an ID signal produced from the base unit.

2. Description of the Prior Art

Recently, many developments have been made on pocket size receivers, for example, cordless telephones, radio pagers or portable telephones, which can effect wireless communication between a base unit and a handset unit.

In these receivers referred to above, portability is particularly emphasized, and accordingly various circuit arrangements are incorporated in a monolithic IC or the like driven by a battery. Thus, from the viewpoint of power saving, a standby mode is presented. When the standby mode is established, the electric power from the battery is supplied to the various circuits intermittently in pulses having a predetermined frequency, so that the handset unit can detect and analyze the ID signal transmitted from the base unit. When the ID signal is detected, the handset unit is changed from the standby mode to the use mode to detect a data signal following the ID signal, thereby starting communication between the handset unit and the base unit. Thus, during the standby mode, the power consumption is saved. Such an arrangement is known from US-A-4 384 361.

An example of a prior art power saving arrangement is shown in Fig. 4.

The circuit shown in Fig. 4 includes a battery 1 which is a power source for the handset unit such as in a cordless phone system, a radio frequency amplifier 2, a mixing circuit 3, a local oscillator 4, an intermediate frequency amplifier 5, a demodulator 6, a signal strength detecting circuit 7 which operates as a detector for detecting the signal level of the received signal, and a waveform shaping circuit 9 for shaping the ID signal from the demodulator 6. A CPU 10 functions to analyze the pattern of received ID signal and to change the mode between standby mode and use mode. During the standby mode, CPU 10 produces a power saving signal PSS to operation control circuit 11 which then produces power in pulses having a predetermined frequency, and supplies the pulsating power to various circuits. Such an intermittent power supply to various circuits is not sufficient to properly process the data signal from the base unit, but is sufficient to analyze the ID signal. Thus, during the standby mode, power necessary to analyze the ID signal is constantly supplied to the various circuits, such as to IF amplifier 5, demodulator 6 and waveshaping circuit 9. When the pattern of the detected ID signal coincides with the pattern stored in CPU 10, the mode is changed from the standby mode to use mode. Under the use mode, the power saving signal PSS is cut off so that the operation control circuit 11 continuously provides the full power to the various circuits.

According to the prior art power saving arrangement, since the intermediate frequency amplifier circuit 5, demodulator circuit 6 and waveform shaping circuit 9 are continuously operated even during the standby mode to analyze the ID signal, there is such a problem that the power consumption during the standby mode is still quite high.

SUMMARY OF THE INVENTION

Accordingly, the present invention has been developed with a view to substantially eliminating the above-described problem in the prior art, and has for its essential object to provide an improved power saving arrangement and power saving method which can further save the power during the standby mode.

In accomplishing these and other objects, a power saving arrangement according to the present invention comprises: a power control circuit for selectively producing a full power and a reduced power; a processing circuit means for receiving and processing said data signal when the full power is applied thereto, and for detecting the level of a received signal when the reduced electric power is applied thereto; detecting circuit means, connected to said processing circuit means, for detecting data signal when the full power is applied thereto, and for detecting only the ID signal when the reduced power is applied thereto; first and second switching means for making and breaking a power supply path to said detecting circuit means from said power control circuit; and control means for controlling said power control circuit and said first switching means to establish either one of first standby mode, second standby mode and use mode such that: in the first standby mode, said first and second switching means break the power supply to said detecting circuit means and, at the same time, the power control circuit produces the reduced power to said processing circuit means, ready to detect the level of said ID signal; in the second standby mode as established when said control means detects that received signal level exceeds a predetermined level, said first and second switching means make the power supply to

said detecting circuit means and, at the same time, the power control circuit produces the reduced power to said processing circuit means and also to said detecting circuit means, ready to detect and read the pattern of said ID signal; and in the use mode as established when said control means detects that said ID signal has a predetermined pattern, said first and second switching means make the power supply to said detecting circuit means and, at the same time, the power control circuit produces the full power to said processing circuit means and also to said detecting circuit means, ready to detect and read said data signal.

Also, according to the present invention, a power saving method comprises the steps of: providing a reduced power to said processing circuit means and providing no power to said detecting circuit means, when ID signal and data signal are not present, ready to detect the level of said received signal by said processing circuit means; providing said reduced power to said processing circuit means and also to said detecting circuit means, when the detected received signal level exceeds a predetermined level, ready to detect the pattern of said ID signal by said detecting circuit means; and providing full power to said processing circuit means and also to said detecting circuit means, when the detected ID signal pattern is identical to a predetermined pattern, ready to detect and reproduce the data signal.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects and features of the present invention will become apparent from the following description taken in conjunction with a preferred embodiment thereof with reference to the accompanying drawings, through which like parts are designated by like reference numerals, and in which:

Fig. 1 is a block diagram of a power saving circuit arrangement according to a preferred embodiment of the present invention;

Fig. 2 is a circuit diagram of a power saving circuit arrangement of Fig. 1;

Fig. 3 is a flow-chart showing the operation of the power saving circuit arrangement of the present invention; and

Fig. 4 is a circuit diagram of a prior art power saving circuit arrangement of a received wave processing circuit.

DESCRIPTION OF PREFERRED EMBODIMENT

Referring to Figs. 1 and 2, a power saving circuit arrangement and the power saving method according to the present invention will be described hereinbelow.

In Figs. 1 and 2, reference numeral 12 represents a radio frequency amplifier circuit for amplifying waves received by an antenna of a cordless phone system or the like; 13 is a mixing circuit for converting high frequency signals to intermediate frequency signals; 14 is a local oscillator; 15 is a first stage intermediate frequency amplifier; 16 is a second stage intermediate frequency amplifier; and 17 is a detector/demodulator for detecting audio signals from the intermediate frequency signals, which are connected in series. Detector/demodulator 17 also produces an ID signal which has been produced from the base unit (not shown) and processed and amplified through circuits 12, 13, 14, 15, 16 and 17. The ID signal from circuit 17 is applied to a CPU 22 in which it is detected whether or not the detected ID signal is the same as the ID signal assigned to the handset unit. Preferably, as shown in Fig. 2, the ID signal is formed by a waveform shaping circuit 25 which filters the output signal from the demodulator 17 and shapes up the waveform.

A signal strength detecting circuit 18 receives signals from first and second stage amplifiers 15 and 16 to generate an RS signal indicative of the strength of the intermediate frequency signals produced from the first and second stage amplifiers 15 and 16. The generated RS signal is applied to CPU 22.

An electric power to each of the circuits 12, 13, 14, 15, 16, 17 and 18 is supplied from a power source 23 through an operation control circuit 24. A power source 23 is, for example, a battery when the processing circuit is employed in a handset unit of a cordless phone system. Furthermore, according to the present invention, the electric power to the second stage amplifiers 16 and modulator 17 are further controlled by first and second switching means 19 and 20, respectively. As diagrammatically shown in Fig. 2, the first switching means 19 includes two switches SW1 and SW2, and the second switching means 20 includes a switch SW3. Also, according to the present invention, the electric power to a portion of signal strength detecting circuit 18 is further controlled by a third switching means 21, which is diagrammatically shown by a switch SW4 in Fig. 2.

CPU 22 produces power saving signals PSS1, PSS2 and PSS3 which are applied to third switching means 21, first and second switching means 19 and 20, and operation control circuit 24, respectively. The power saving signals PSS1 and PSS2 control ON/OFF operations of the first and second switching means 19 and 20, and the power saving signal PSS3 controls operation control circuit 24 such that operation control circuit 24 generates an intermittent operating voltage +Vcc in pulses having a predetermined frequency when the power

saving signal PSS3 is present, but it generates a continuous operating voltage +Vcc when the power saving signal PSS3 is not present.

By using the RS signal and ID signal, CPU 22 determines the mode which is either a first standby mode, a second standby mode or a use mode.

The operation of the power saving circuit shown in Figs. 1 and 2 will be described hereinbelow with reference to the flow chart of Fig. 3. In Fig. 3, the operation under the first standby mode is indicated by MD1 covering steps P1-P3, the second standby mode by MD2 covering steps P4 and P5, and the use mode by MD3 covering steps P6-P8, respectively.

Under the first standby mode MD1, power saving signals PSS1, PSS2 and PSS3 are produced. Thus, at step P1, by the power saving signal PSS2, the first and second switching means 19 and 20 are both turned off so that the electric power from the operation control circuit 24 to each of second stage intermediate frequency amplifier 16 and detector/demodulator 17 is cut off. Also, by the power saving signal PSS1, the third switching means 21 is turned off so that the electric power to the portion of signal strength detecting circuit 18 is cut off.

Then at step P2, by the power saving signal PSS3, operation control circuit 24 is so operated as to produce pulsating power at a predetermined frequency (also referred to as an intermittent voltage (+Vcc) power). Thus, first stage intermediate frequency amplifier 15, mixing circuit 13, local oscillator 14 and radio frequency amplifier circuit 12 and a portion of signal strength detecting circuit 18 are operated intermittently.

Thus, under the first standby mode MD1, no power is consumed in circuits 16 and 17 and reduced power is consumed in circuits 12, 13, 14, 15 and 18, the rate of reduction being dependent on the duty ratio of the intermittent voltage power as set in operation control circuit 24. Accordingly, by the half powered circuits 12, 13, 14, 15 and 18, the signal received by the antenna will not be processed properly, but is processed sufficiently to detect the level of the received signal. Such a detection of the received signal level is carried out particularly in signal strength detecting circuit 18 which then produces RS signal representing the received signal level.

At step P3, it is detected in CPU 22 using the RS signal whether or not the received signal level is greater than a predetermined level. If no signal is being received or if the receiving signal level is lower than the predetermined level because, e.g., the handset unit is far from the base station, step P3 for the detection of RS signal is repeated. On the contrary, if it is detected that the received signal level is greater than the predetermined level, the program advances to step P4 to enter the second standby mode MD2.

Under the second standby mode, power saving signals PSS1 and PSS2 are stopped and only the power saving signal PSS3 is applied to operation control circuit 24.

Thus, at step P4, by the absence of power saving signals PSS1 and PSS2, the first and second switching means are turned on to permit intermittent voltage (+Vcc) power supply from power control circuit 24 to second stage amplifier 16 and to detector/demodulator 17. Thus, at this point, all the circuits 12, 13, 14, 15, 16, 17 and 18 are provided with intermittent voltage (+Vcc) power from circuit 24. Such a reduced power is not sufficient to properly detect and reproduce the audio signals, but is sufficient to properly detect and reproduce ID signal which is applied to CPU 22. Then, at step P5, it is detected in CPU 22 whether or not the received ID signal has a pattern which is identical to the ID signal pattern assigned to that handset unit. If the ID signal pattern does not match, the program returns to step P1 to start from the first standby mode. If the ID signal pattern does match, the program advances to step P6 to enter the use mode.

Under the use mode, all the power saving signals PSS1, PSS2 and PSS3 are stopped. By the absence of power saving signals PSS1 and PSS2, the first, second and third switching circuits are turned on, and by the absence of power saving signal PSS3, operation control circuit 24 is so operated as to produce full power, i.e., continuous voltage (+Vcc) power. Thus, circuits 12, 13, 14, 15, 16, 17 and 18 are operated with full power to properly detect and generate the received audio signal, thereby enabling communication between the base unit and the handset unit at step P7. When the communication ends (step P8), the program returns to step P1 to start the first standby mode.

Thus, in the manner as described hereinabove, the power saving operation is effected in two different levels, i.e., the high percentage saving as effected under the first standby mode MD1, and low percentage saving as effected under the second standby mode MD2.

More specifically, under the first standby mode MD1, that is, when no signal is received or when the received signal is weak, only circuits 12, 13, 14 and 15 and a portion of circuit 18 are operated with about half or less power, depending on the duty ratio of the pulsating voltage (+Vcc) power, which is sufficient to receive and detect the level of the ID signal. Thus, under the first standby mode MD1, the power for operating circuits 16 and 17 is saved, and also some percentage of power for operating circuits 12, 13, 14, 15 and 18 is saved.

Under the second standby mode MD2, that is, when the received signal has a sufficiently large strength, circuits 12, 13, 14, 15, 16, 17 and 18 are operated with about half or less power, which is sufficient to detect and read the ID signal pattern. Thus, under the second standby mode MD2, some percentage of power for operating circuits 12 to 18 is saved.

As has been described hereinabove, according to the present invention, since the receiving mode is divided into three modes, the power consumption can be reduced to a large extent, and the life time of the battery can be prolonged.

Although the present invention has been fully described by way of example with reference to the accompanying drawings, it is to be noted here that various changes and modifications would be apparent to those skilled in the art. Therefore, unless otherwise such changes and modifications depart from the scope of the claims of the present invention, they should be construed as included therein.

Claims

1. A power saving arrangement for use in a subsidiary unit which communicates with a base unit in response to the detection of an ID signal leading data signal which are produced from said base unit and received by said subsidiary unit, said power saving arrangement comprising:

   a power control circuit (23, 24) for selectively producing a full power and a reduced power;

   a processing circuit means (12, 13, 14, 15, 18) for receiving and processing said data signal when the full power is applied thereto, and for detecting the level of the received signal when the reduced electric power is applied thereto;

   detecting circuit means (16, 17), connected to said processing circuit means, for detecting data signal when the full power is applied thereto, and for detecting only the ID signal when the reduced power is applied thereto;

   first and second switching means (SW1, SW2, SW3) for making and breaking a power supply path to said detecting circuit means from said power control circuit; and

   control means (CPU) for controlling said power control circuit and said first switching means to establish either one of first standby mode, second standby mode and use mode such that:

   in the first standby mode, said first and second switching means (SW1, SW2, SW3) break the power supply to said detecting circuit means (16, 17) and, at the same time, the power control circuit (23, 24) produces the reduced power to said processing circuit means (12, 13, 14, 15, 18), ready to detect the level of the received signal;

   in the second standby mode as established when said control means (CPU) detects that the received signal level exceeds a predetermined level, said first and second switching means (SW1, SW2, SW3) make the power supply to said detecting circuit means (16, 17) and, at the same time, the power control circuit (23, 24) produces the reduced power to said processing circuit means and also to said detecting circuit means, ready to detect and read the pattern of said ID signal; and

   in the use mode as established when said control means (CPU) detects that said ID signal has a predetermined pattern, said first and second switching means (SW1, SW2, SW3) make the power supply to said detecting circuit means (16, 17) and, at the same time, the power control circuit (23, 24) produces the full power to said processing circuit means (12, 13, 14, 15, 18) and also to said detecting circuit means (16, 17), ready to detect and read said data signal.

2. A power saving arrangement as claimed in Claim 1, wherein said processing circuit means (12, 13, 14, 15, 18) comprises a signal strength detecting circuit (18) for detecting the signal level of the received signal.

3. A power saving arrangement as claimed in Claim 2, further comprising a third switching means (SW4) which operates synchronously with said first switching means (SW1, SW2, SW3) for making and breaking power supply to said signal strength detecting circuit (18).

4. A power saving arrangement as claimed in Claim 1, wherein said processing circuit means comprises a first stage amplifier (15).

5. A power saving arrangement as claimed in Claim 1, wherein said detecting circuit means comprises a second stage amplifier (16) and a detector/modulator circuit (17).

6. A power saving arrangement as claimed in Claim 1, wherein said control means comprises a CPU.

7. A power saving arrangement as claimed in Claim 1, wherein said power control circuit comprises an operation control (24) for producing said full power or said reduced power.

8. A power saving arrangement as claimed in Claim 7, wherein said operation control (24) produces power intermittently thereby generating said reduced power.

9. A power saving method for use in a subsidiary unit which communicates with a base unit in response to the detection of an ID signal leading data signal which is produced from said base unit, said subsidiary unit having a processing circuit means (12, 13, 14, 15, 18) for receiving and processing said ID signal and data signal, and a detecting circuit means (16, 17), connected to said processing circuit means, for detecting said ID signal and data signal, the power saving method comprising the steps of:

providing a reduced power to said processing circuit means (12, 13, 14, 15, 18) and providing no power to said detecting circuit means (16, 17), when said ID signal and data signal are not present, ready to detect the level of the received signal by said processing circuit means;

providing said reduced power to said processing circuit means (12, 13, 14, 15, 18) and also to said detecting circuit means (16, 17), when the detected received signal level exceeds a predetermined level, ready to detect the pattern of said ID signal by said detecting circuit means; and

providing full power to said processing circuit means (12, 13, 14, 15, 18) and also to said detecting circuit means (16, 17), when the detected ID signal pattern is identical to a predetermined pattern, ready to detect and reproduce the data signal.

10. A power saving method as claimed in Claim 9, wherein said reduced power is produced by intermittently generating the power.

Patentansprüche

1. Leistungssparanordung zur Verwendung in einer Untereinheit, die mit einer Basiseinheit in Abhängigkeit von der Erfassung eines Identifikationssignals kommuniziert, das einem Datensignal vorausgeht, wobei die Signale von der Basiseinheit erzeugt und von der Untereinheit empfangen werden, wobei die Leistungssparanordnung aufweist:

eine Leistungssteuerschaltung (23, 24) zum selektiven Erzeugen voller Leistung und reduzierter Leistung,

eine Verarbeitungsschaltungseinrichtung (12, 13, 14, 15, 18) zum Empfangen und Verarbeiten des Datensignals, wenn ihr vollständige Leistung zugeführt wird, und zur Erfassung des Pegels des empfangenen Signals, wenn ihr reduzierte elektrische Leistung zugeführt wird,

eine Detektorschaltungseinrichtung (16, 17), die mit der Verarbeitungsschaltungeinrichtung verbunden ist, zur Erfassung eines Datensignals, wenn ihr Volleistung zugeführt wird, und zur Erfassung nur des Identifikationssignals, wenn ihr reduzierte Leistung zugeführt wird, eine ersten und einer zweiten Schalteinrichtung (SW1, SW2, SW3) zur Herstellung und Unterbrechung eines Leistungszufuhrweges an die Detektorschaltungseinrichtung von der Leistungssteuerschaltung und

eine Steuereinrichtung (CPU) zur Steuerung der Leistungssteuerschaltung und der ersten Schalteinrichtung zur Einstellung eines Modus aus einem ersten Bereitschaftsmodus, einem zweiten Bereitschaftsmodus und einem Benutzungsmodus derart, daß:

im ersten Bereitschaftsmodus die erste und die zweite Schalteinrichtung (SW1, SW2, SW3) die Leistungszufuhr an die Detektorschaltungseinrichtung (16, 17) unterbrechen und gleichzeitig die Leistungssteuerschaltung (23, 24) die reduzierte Leistung für die Verarbeitungsschaltungseinrichtung (12, 13, 14, 15, 18) erzeugt, die bereit ist, den Pegel des empfangenen Signals zu erfassen,

im zweiten Bereitschaftsmodus, der eingestellt ist, wenn die Steuereinrichtung (CPU) erfaßt, daß der empfangene Signalpegel einen vorgegebenen Pegel überschreitet, die erste und die zweite Schalteinrichtung (SW1, SW2, SW3) die Leistungszufuhr an die Detektorschaltungseinrichtung (16, 17) herstellt und gleichzeitig die Leistungssteuerschaltung (23, 24) die reduzierte Leistung für die Verarbeitungsschaltungeinrichtung und ebenfalls für die Detektorschaltungseinrichtung erzeugt, die bereit sind, das Muster des Identifikationssignals zu erfassen und zu lesen, und

im Benutzungsmodus, der hergestellt wird, wenn die Steuereinrichtung (CPU) erfaßt, daß das Identifikationssignal ein vorgegebenes Muster aufweist, die erste und die zweite Schalteinrichtung (SW1, SW2, SW3) die Leistungszufuhr an die Detektorschaltungseinrichtung (16, 17) herstellen und gleichzeitig die Leistungssteuerschaltung (23, 24) die volle Leistung für die Verarbeitungsschaltungseinrichtung (12, 13, 14, 15, 18) und ebenfalls für die Detektorschaltungseinrichtung (16, 17) erzeugt, die bereit sind, das Datensignal zu erfassen und zu lesen.

2. Leistungssparanordnung nach Anspruch 1, wobei die Verarbeitungschaltungseinrichtung (12,

13, 14, 15, 18) eine Signalstärken-Erfassungsschaltung (18) aufweist zur Erfassung des Signalpegels des empfangenen Signals.

3. Leistungssparanordnung nach Anspruch 2, mit ferner einer dritten Schalteinrichtung (SW4), die synchron mit der ersten Schalteinrichtung (SW1, SW2, SW3) arbeitet zur Herstellung und Unterbrechung der Leistungszufuhr an die Signalstärken-Detektorschaltungen (18).

4. Leistungssparanordnung nach Anspruch 1, bei der die Verarbeitungsschaltungseinrichtung einen Erststufenverstärker (15) aufweist.

5. Leistungssparanordnung nach Anspruch 1, wobei die Detektorschaltungseinrichtung einen Zweitstufenverstärker (16) und eine Detektor/Modulatorschaltung (17) aufweist.

6. Leistungssparanordnung nach Anspruch 1, wobei die Steuereinrichtung eine CPU aufweist.

7. Leistungssparanordnung nach Anspruch 1, wobei die Leistungssteuerschaltung eine Betriebssteuerung (24) zur Erzeugung der vollen Leistung und der reduzierten Leistung aufweist.

8. Leistungssparanordnung nach Anspruch 7, wobei die Betriebssteuerung (24) intermittierend Leistung erzeugt, wodurch die reduzierte Leistung erzeugt wird.

9. Leistungssparverfahren zur Verwendung in einer Untereinheit, die mit einer Basiseinheit in Abhängigkeit von der Erfassung eines Identifikationssignals kommuniziert, das einem Datensignal vorausgeht, wobei die Signale von der Basiseinheit erzeugt werden, wobei die Untereinheit eine Verarbeitungsschaltungseinrichtung (12, 13, 14, 15, 18) aufweist zum Empfang und zum Verarbeiten des Identifikationssignals und des Datensignals und eine Detektorschaltungseinrichtung (16, 17), die mit der Verarbeitungsschaltungseinrichtung verbunden ist, zur Erfassung des Identifikationssignals und des Datensignals, wobei das Leistungssparverfahren die Schritte aufweist:

Zuführung einer reduzierten Leistung an die Verarbeitungsschaltungseinrichtung (12, 13, 14, 15, 18) und Nichtzuführung von Leistung an die Detektorschaltungseinrichtung (16, 17), wenn das Identifikationssignal und das Datensignal nicht vorhanden sind, zur Erfassung des Pegels des empfangenen Singal durch die Verarbeitungsschaltungseinrichtung,

Zuführung der reduzierten Leistung an die Verarbeitungsschaltungseinrichtung (12, 13, 14, 15, 18) und ebenfalls an die Detektorschaltungseinrichtung (16, 17), wenn der erfaßte empfangene Signalpegel einen vorgegebenen Pegel überschreitet, zur Erfassung des Musters des Identifikationssignals durch die Detektorschaltungseinrichtung, und

Zuführung voller Leistung an die Verarbeitungsschaltungseinrichtung (12, 13, 14, 15, 18) und ebenfalls an die Detektorschaltungseinrichtung (16, 17), wenn das erfaßte Identifikationssignalmuster identisch einem vorgegebenen Muster ist, zur Erfassung und zur Wiedergabe des Datensignals.

10. Leistungssparverfahren nach Anspruch 9, wobei die reduzierte Leistung durch das intermittierende Erzeugen der Leistung hergestellt wird.

Revendications

1. Agencement d'économie de puissance pour une unité auxiliaire communiquant avec une unité de base en réponse à la détection d'un signal ID précédant un signal de données qui sont produits par ladite unité de base et sont reçus par ladite unité auxiliaire, ledit agencement d'économie de puissance comprenant :
   - un circuit de commande de puissance (23, 24) pour produire, de façon sélective, une pleine puissance et une puissance réduite;
   - un moyen de circuit de traitement (12, 13, 14, 15, 18) pour recevoir et pour traiter ledit signal de données lors de l'application de la pleine puissance et pour détecter le niveau du signal reçu lors de l'application de la puissance électrique réduite;
   - un premier et un second moyens de commutation (SW1, SW2, SW3) pour établir et pour fermer un circuit d'alimentation de puissance vers ledit moyen de circuit de détection à partir dudit circuit de commande de puissance; et
   - un moyen de commande (CPU) dudit circuit de commande de puissance et dudit premier moyen de commutation pour établir un quelconque parmi un premier mode d'attente, un second mode d'attente et un mode d'utilisation de telle façon que :
   - dans le premier mode d'attente, lesdits premier et second moyens de commutation (SW1, SW2, SW3) ferment l'alimentation de puissance vers ledit moyen de circuit de détection (16, 17) et, en même temps, le circuit de commande de puis-

sance produit la puissance réduite vers ledit moyen de circuit de traitement (12, 13, 14, 15, 18), prêts à détecter le niveau dudit signal ID;

- dans le second mode d'attente tel qu'établi lorsque ledit moyen de commande (CPU) détecte que le niveau du signal reçu dépasse un niveau prédéterminé, lesdits premier et second moyens de commutation (SW1, SW2, SW3) établissent l'alimentation de puissance vers ledit moyen de circuit de détection (16, 17) et, en même temps, le circuit de commande de puissance (23, 24) produit la puissance réduite vers ledit moyen de circuit de traitement (12, 13, 14, 15, 18) et de même, vers ledit moyen de circuit de détection (16, 17), prêts à détecter et à lire la configuration dudit signal ID; et
- dans le mode d'utilisation comme établi lorsque ledit moyen de commande (CPU) détecte que ledit signal ID présente une configuration prédéterminée, lesdits premier et second moyens de commutation (SW1, SW2, SW3) établissent l'alimentation de puissance vers ledit moyen de circuit de détection (16, 17) et en même temps, le circuit de commande de puissance (23, 24) produit la pleine puissance vers ledit moyen de circuit de traitement (12, 13, 14, 15, 18) et, de même, vers ledit moyen de circuit de détection (16, 17), prêts à détecter et à lire ledit signal de données.

2. Agencement d'économie de puissance selon la revendication 1, dans lequel ledit moyen de circuit de traitement (12, 13, 14, 15, 18) comprend un circuit de détection d'amplitude du signal (18) pour détecter le niveau du signal reçu.

3. Agencement d'économie de puissance selon la revendication 2, comprenant, de plus, un troisième moyen de commutation (SW4) fonctionnant, de façon synchrone, avec ledit premier moyen de commutation (SW1, SW2, SW3) pour établir et pour fermer l'alimentation de puissance vers ledit circuit de détection d'amplitude du signal (18).

4. Agencement d'économie de puissance selon la revendication 1, dans lequel ledit moyen de circuit de traitement (12, 13, 14, 15, 18) comprend un amplificateur de première étage (15).

5. Agencement d'économie de puissance selon la revendication 1, dans lequel ledit moyen de circuit de détection (16, 17) comprend un amplificateur de second étage (16) et un circuit de détecteur/modulateur (17).

6. Agencement d'économie de puissance selon la revendication 1, dans lequel ledit moyen de commande comprend une CPU.

7. Agencement d'économie de puissance selon la revendication 1, dans lequel ledit circuit de commande de puissance (23, 24) comprend une commande de fonctionnement (24) pour produire ladite pleine puissance ou ladite puissance réduite.

8. Agencement d'économie de puissance selon la revendication 7, dans lequel ladite commande de fonctionnement (24) produit une puissance intermittente, générant ainsi ladite puissance réduite.

9. Procédé d'économie de puissance pour une unité auxiliaire communiquant avec une unité de base en réponse à la détection d'un signal ID précédant un signal de données produit par ladite unité de base, ladite unité auxiliaire possédant un moyen de circuit de traitement (12, 13, 14, 15, 18) pour recevoir et traiter ledit signal ID et ledit signal de données et un moyen de circuit de détection (16, 17) raccordé audit moyen de circuit de traitement (12, 13, 14, 15, 18) pour la détection dudit signal ID et dudit signal de données;

procédé d'économie de puissance comprenant les étapes suivantes :

- la fourniture d'une puissance réduite audit circuit de traitement (12, 13, 14, 15, 18) et aucune puissance audit circuit de détection (16, 17) lorsque le signal ID et le signal de données ne sont pas présents, circuits prêts à détecter le niveau dudit signal reçu par ledit circuit de traitement (12, 13, 14, 15, 18);
- la fourniture de ladite puissance réduite audit circuit de traitement (12, 13, 14, 15, 18) et, de même, audit circuit de détection (16, 17) lorsque le niveau détecté du signal reçu dépasse un niveau prédéterminé, circuits prêts à détecter la configuration dudit signal ID par ledit circuit de détection (16, 17); et
- la fourniture de la pleine puissance audit circuit de traitement (12, 13, 14, 15, 18) et, de même, audit circuit de détection (16, 17) lorsque la configuration détectée du signal ID est identique à une configuration prédéterminée, circuits prêts à détecter et à lire le signal de données.

10. Procédé d'économie de puissance selon la revendication 9, selon lequel ladite puissance réduite est produite par génération intermittente de la puissance.

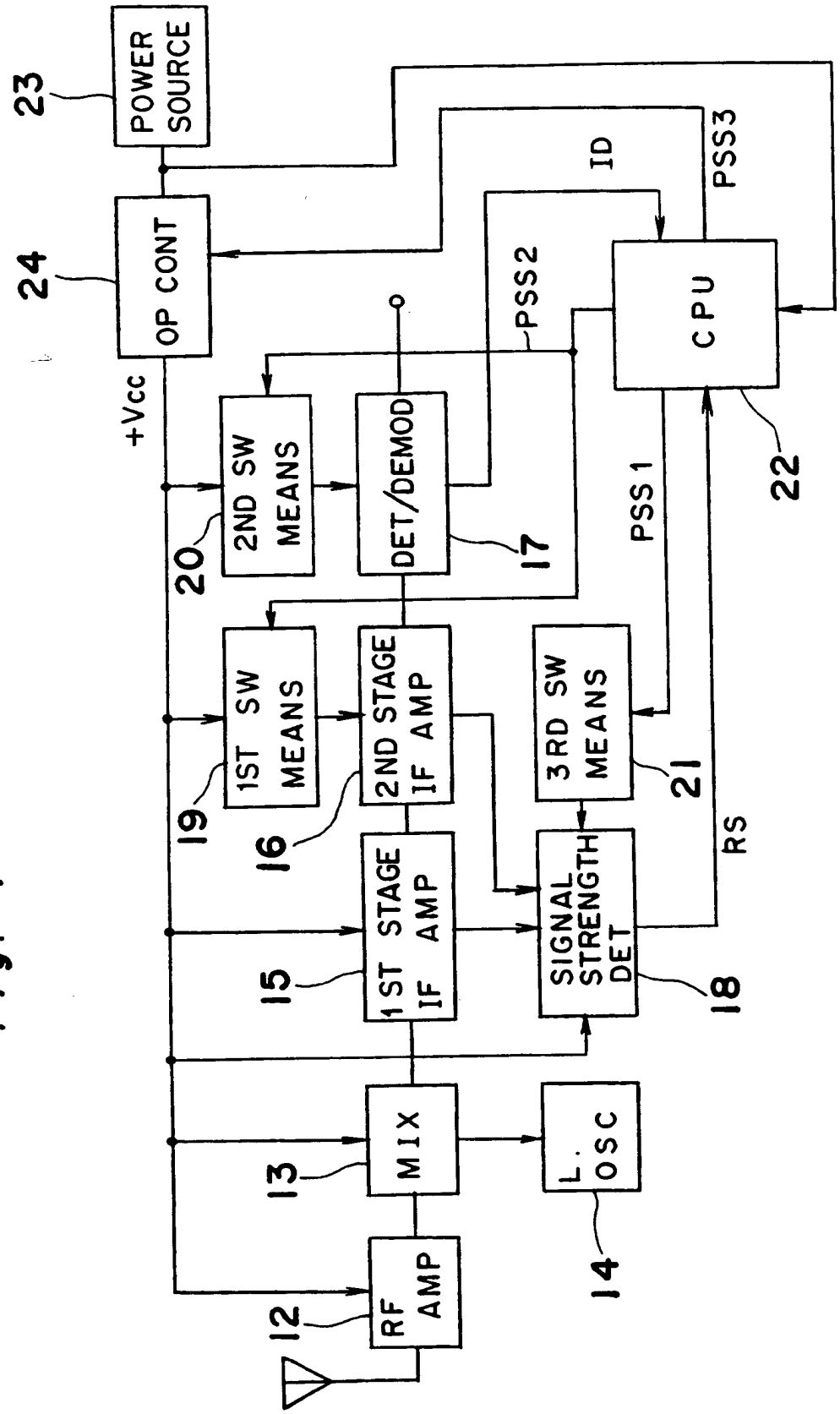


Fig. 1

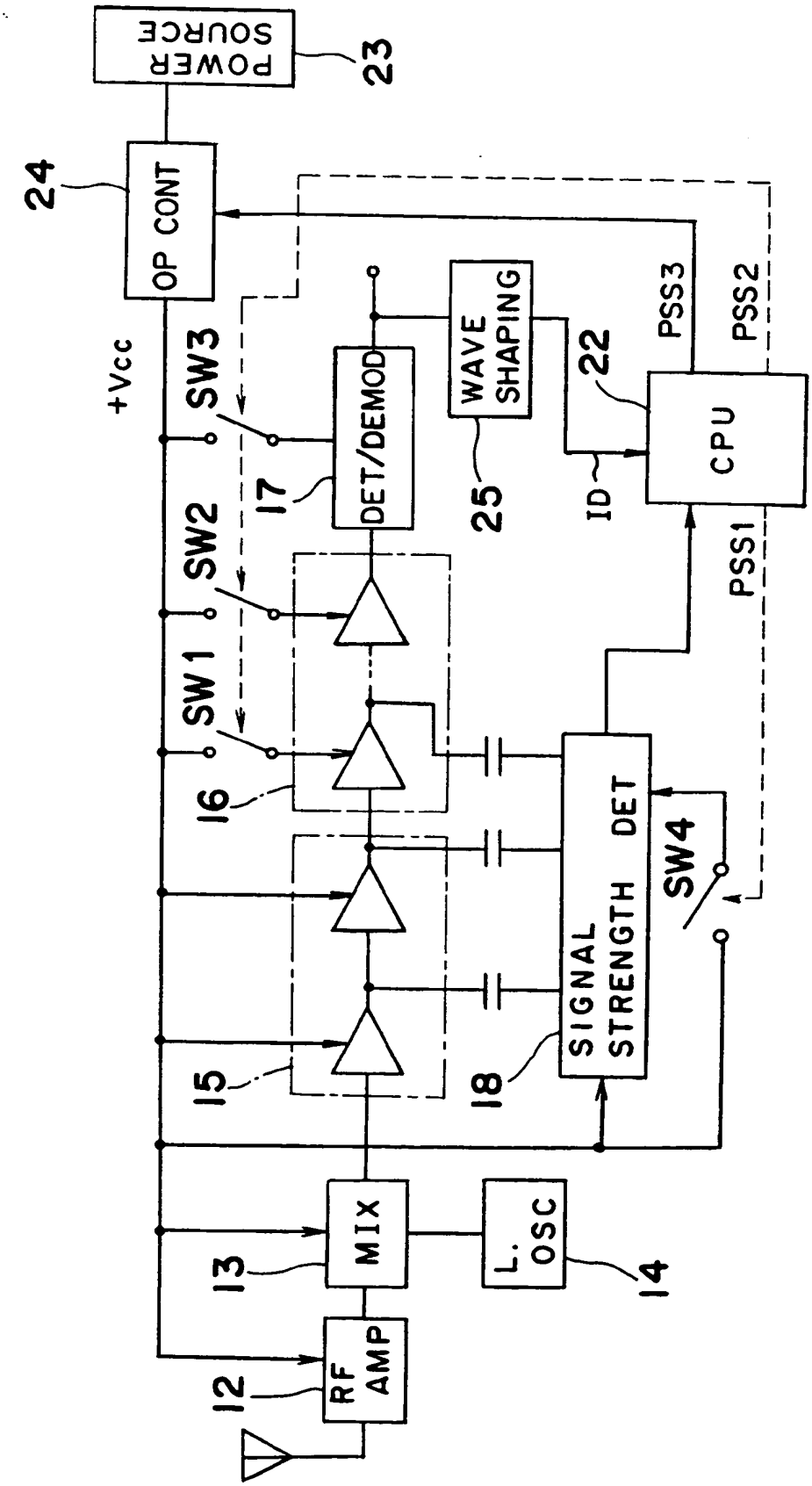
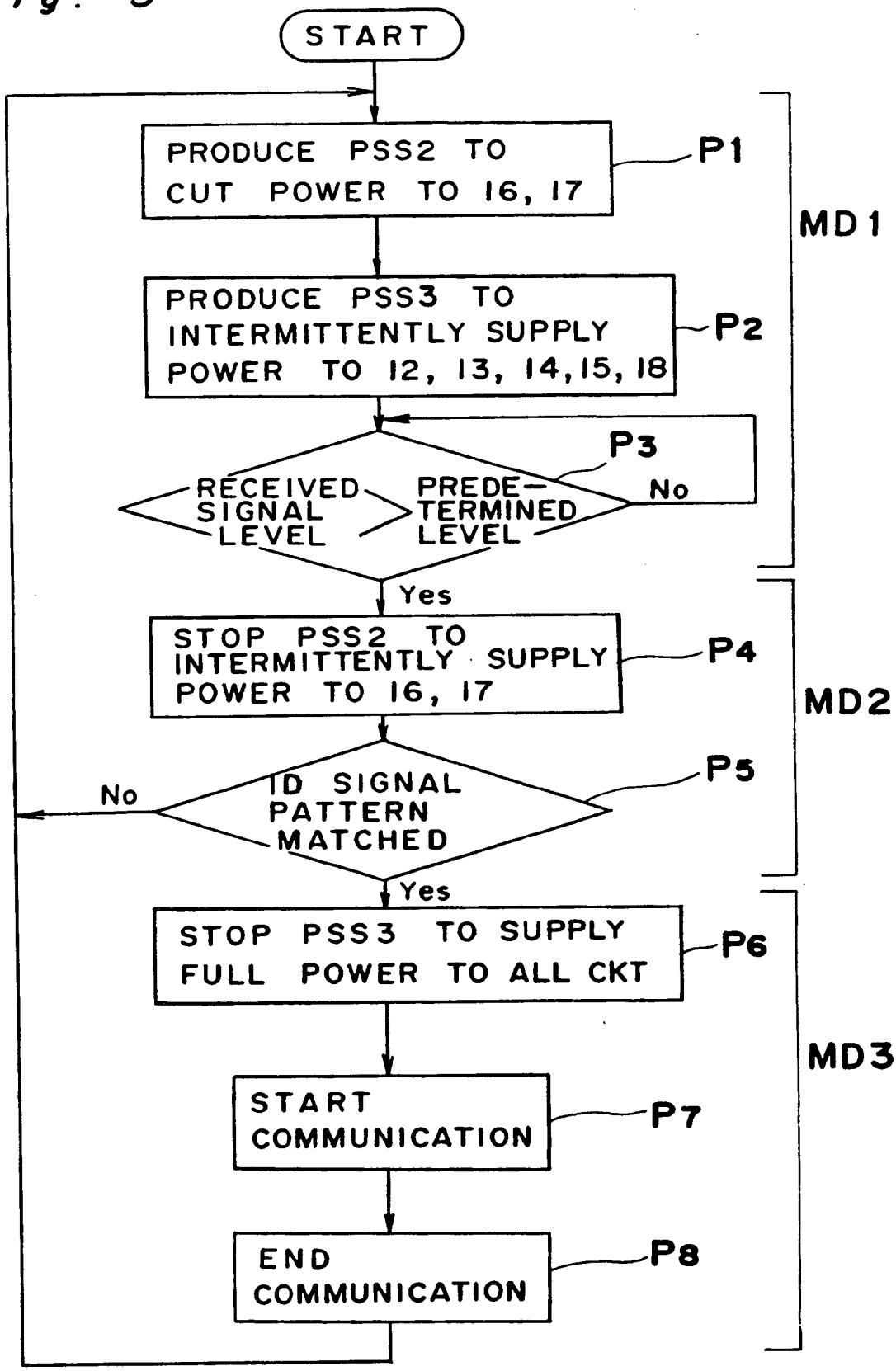

POWER SOURCE
23
24
OP CONT
+Vcc
SW3
SW2
SW1
DET/DEMOD
17
WAVE SHAPING
25
22
ID
CPU
PSS3
PSS2
PSS1
16
15
SIGNAL STRENGTH DET
18
SW4
MIX
13
L. OSC
14
RF AMP
12

Fig. 2

Fig. 3



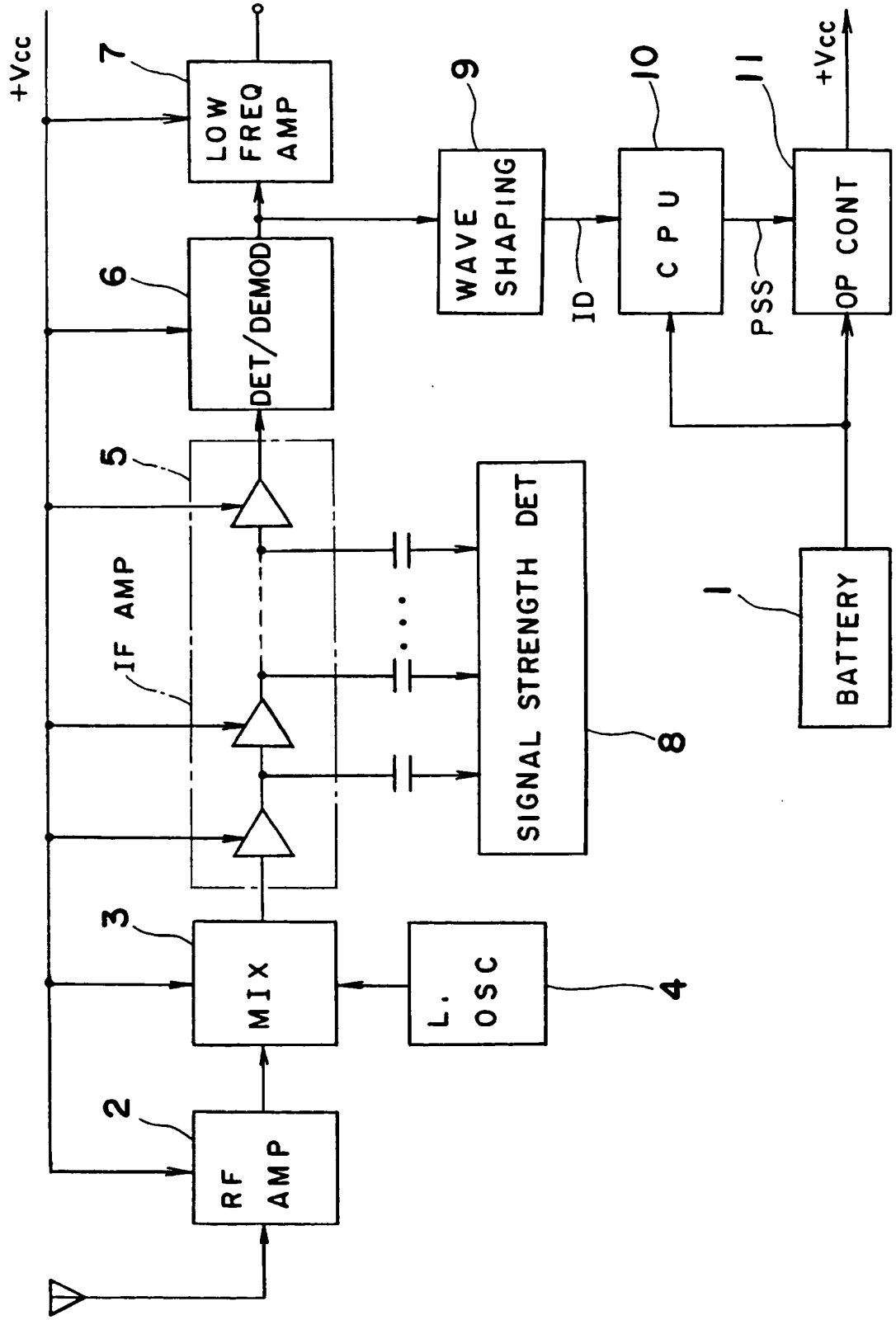


Fig. 4 PRIOR ART